REMARKS

This Amendment is being filed in response to the Office Action dated November 4, 2004. For the following reasons, this application should be considered in condition for allowance and the case passed to issue.

Claims 1-15 were objected to for informalities. These informalities have been corrected by the amendments made to address the specific concerns raised by the Examiner. However, the Examiner objected to claims 3, 8, 12 and 14, stating that the recitation of "3 sigma via-to-metal size" is not clear as to what Applicants intend to mean. It is respectfully noted that the term "3 sigma", as it relates to errors, is a statistical measure well known in the art of semiconductor layout technology. For example, see U.S. Patent No. 6,108,623, in which the term "3 sigma" is used extensively throughout the claims and specification. Other examples may be provided should the Examiner require. Hence, the term "3 sigma via-to-metal size and positioning error factor" is one that a person of ordinary skill in the art would readily recognize and understand.

For the above reasons, reconsideration and withdrawal of the objection to claims 1-15 are respectfully requested.

The indication of allowability of claims 4-7 and the allowance of claims 8-12 and 14 is gratefully acknowledged. However, at this time in light of the amendments and remarks above, claims 4-7 have not been incorporated into independent claim 1.

Claims 1-3, 13 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eden et al. (hereafter "Eden"). The following is a comparison of the present invention as currently claimed with the Eden reference.

The present invention, as recited in claim 1, for example, relates to a method for generating a circuit layout comprising the steps of selecting at least one via that has at least one

edge touching an edge of an overlying metal line, and measuring a distance between the edge of the overlying metal line and an edge of an adjacent metal line. When the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is at least a predetermined distance, then a width of the overlying metal line is increased. However, if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, then the width of the overlying metal line is increased and the width of the adjacent metal line is decreased. The cited references neither show nor suggest the invention as now claimed.

Eden, U.S. Patent No. 5,620, 916, relates to a method for improving via/contact coverage in an integrated circuit. The Examiner conceded that Eden lacks a method/apparatus/program in which if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, then the size of the overlying metal line is increased and the size of the adjacent metal line is decreased. However, it is considered obvious by the Examiner to employ Eden's teaching regarding the method/apparatus/program by employing the CAD tool in the manner claimed. The stated reason was in order to keep the minimum distance between the increased size of the contact area and adjacent metal line according to the predetermined distance. However, it was respectfully submitted that this particular claimed solution of the present invention is not obvious, and there is nothing in Eden that would lead one of ordinary skill in the art towards maintaining a minimum distance in this manner. In fact, Eden provides its own methodology for design rule violations. As discussed in column 3, lines 1-20, an initial layout is generated wherein the individual interconnect lines of the interconnect layer are separated by at least the minimum distance. The overlap of each side of each via by interconnect lines is increased to a first predetermined amount. Next, the overlap

of each side of each via is checked to determined if increasing the overlap of the first predetermined amount violates a design rule. If a side of a via does violate a design rule, the first predetermined amount of overlap is removed from those sides of those vias which violate the design rule. Next, a second, smaller amount of overlap is provided to those sides of those vias which violated the design rule when increased to the first predetermined amount. The second predetermined amount of overlaps are then checked to determine if any of the second, smaller overlaps violate the design rule. If so, those overlaps are removed. This process is continued in this manner until there are no design rule violations.

Eden therefore accommodates the situation in which the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, by a completely different methodology. After increasing the size of a first line, and then determining that a design rule has been violated, Eden reduces the size of the overlap of this via in the first line, without performing any reduction whatsoever in the second line. This compromises the security of the via and line overlap connection, especially as compared to the present invention in which the reduction is not taken in the line overlapping the via, but rather in the line that does not have the via at the point of design violation (where the distance is less than a predetermined distance). The present invention thus takes an unobvious approach to design violation remedy, by reducing the line which has not been increased in size, rather than merely lessening the amount of size increase in the line that has already been increased. There is nothing in Eden that suggests that the approach of the present invention should replace the approach already provided by Eden, nor why one of ordinary skill in the art would be lead by Eden to discard their disclosed approach.

Accordingly, since Eden fails to show or remotely suggest the claimed methodology of the present invention, the rejection of claims 1-3, 13 and 15 under 35 U.S.C. § 103(a) should be reconsidered and withdrawn. Such action is courteously solicited.

In light of the Amendments and Remarks above, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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